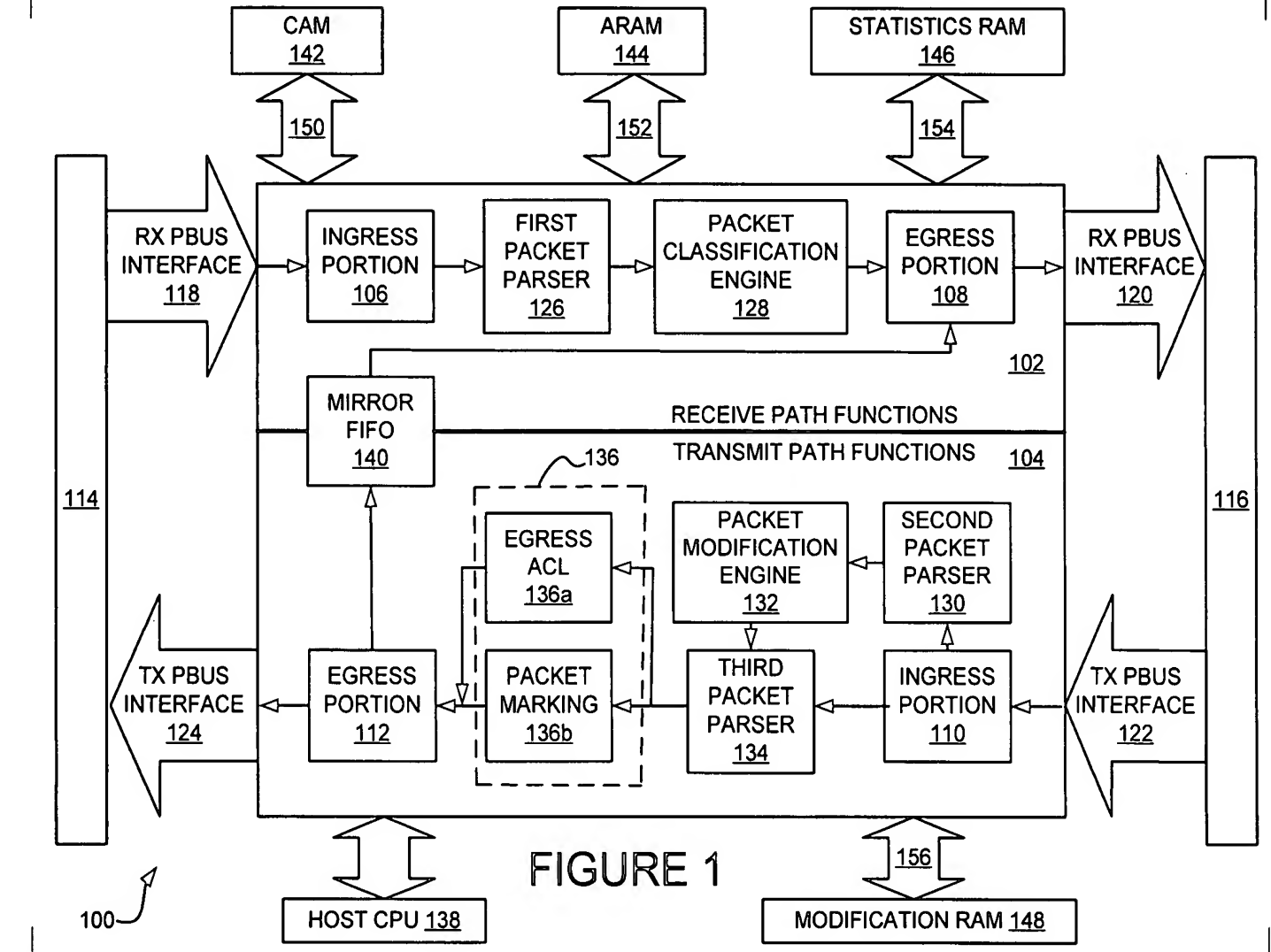
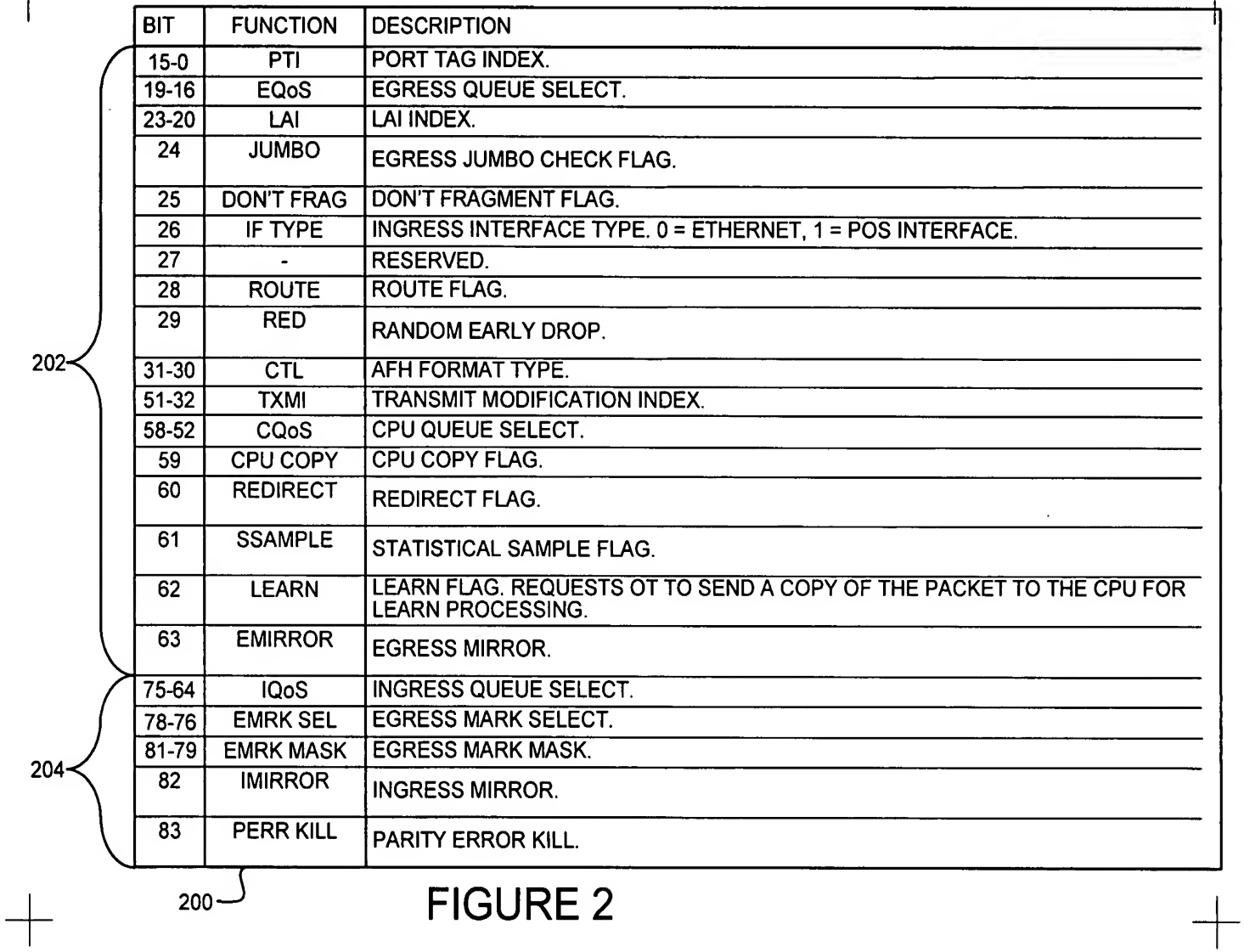

CAM
142
ARAM
144
STATISTICS RAM
146
150
152
154
RX PBUS
INTERFACE
118
INGRESS
PORTION
106
FIRST
PACKET
PARSER
126
PACKET
CLASSIFICATION
ENGINE
128
EGRESS
PORTION
108
RX PBUS
INTERFACE
120
102
MIRROR
FIFO
140
RECEIVE PATH FUNCTIONS
TRANSMIT PATH FUNCTIONS
104
136
114
116
EGRESS
ACL
136a
PACKET
MODIFICATION
ENGINE
132
SECOND
PACKET
PARSER
130
TX PBUS
INTERFACE
124
EGRESS
PORTION
112
PACKET
MARKING
136b
THIRD
PACKET
PARSER
134
INGRESS
PORTION
110
TX PBUS
INTERFACE
122
156
100
HOST CPU 138
MODIFICATION RAM 148

FIGURE 1



BIT	FUNCTION	DESCRIPTION
15-0	PTI	PORT TAG INDEX.
19-16	EQoS	EGRESS QUEUE SELECT.
23-20	LAI	LAI INDEX.
24	JUMBO	EGRESS JUMBO CHECK FLAG.
25	DON'T FRAG	DON'T FRAGMENT FLAG.
26	IF TYPE	INGRESS INTERFACE TYPE. 0 = ETHERNET, 1 = POS INTERFACE.
27	-	RESERVED.
28	ROUTE	ROUTE FLAG.
29	RED	RANDOM EARLY DROP.
31-30	CTL	AFH FORMAT TYPE.
51-32	TXMI	TRANSMIT MODIFICATION INDEX.
58-52	CQoS	CPU QUEUE SELECT.
59	CPU COPY	CPU COPY FLAG.
60	REDIRECT	REDIRECT FLAG.
61	SSAMPLE	STATISTICAL SAMPLE FLAG.
62	LEARN	LEARN FLAG. REQUESTS OT TO SEND A COPY OF THE PACKET TO THE CPU FOR LEARN PROCESSING.
63	EMIRROR	EGRESS MIRROR.
75-64	IQoS	INGRESS QUEUE SELECT.
78-76	EMRK SEL	EGRESS MARK SELECT.
81-79	EMRK MASK	EGRESS MARK MASK.
82	IMIRROR	INGRESS MIRROR.
83	PERR KILL	PARITY ERROR KILL.

FIGURE 2

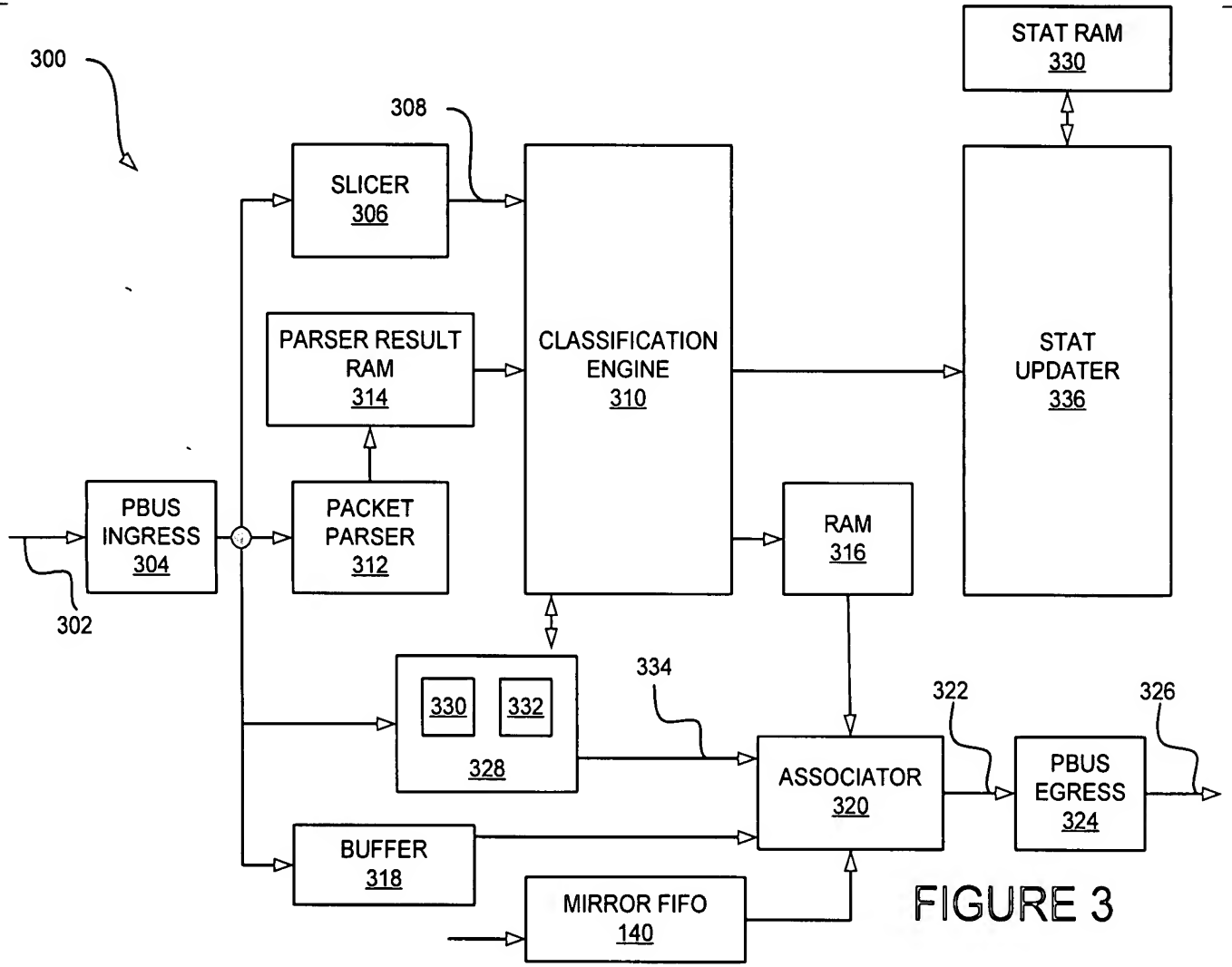

300
308
SLICER
306
STAT RAM
330
PARSER RESULT
RAM
314
CLASSIFICATION
ENGINE
310
STAT
UPDATER
336
PBUS
INGRESS
304
PACKET
PARSER
312
RAM
316
302
330
332
328
334
322
326
ASSOCIATOR
320
PBUS
EGRESS
324
BUFFER
318
MIRROR FIFO
140

FIGURE 3

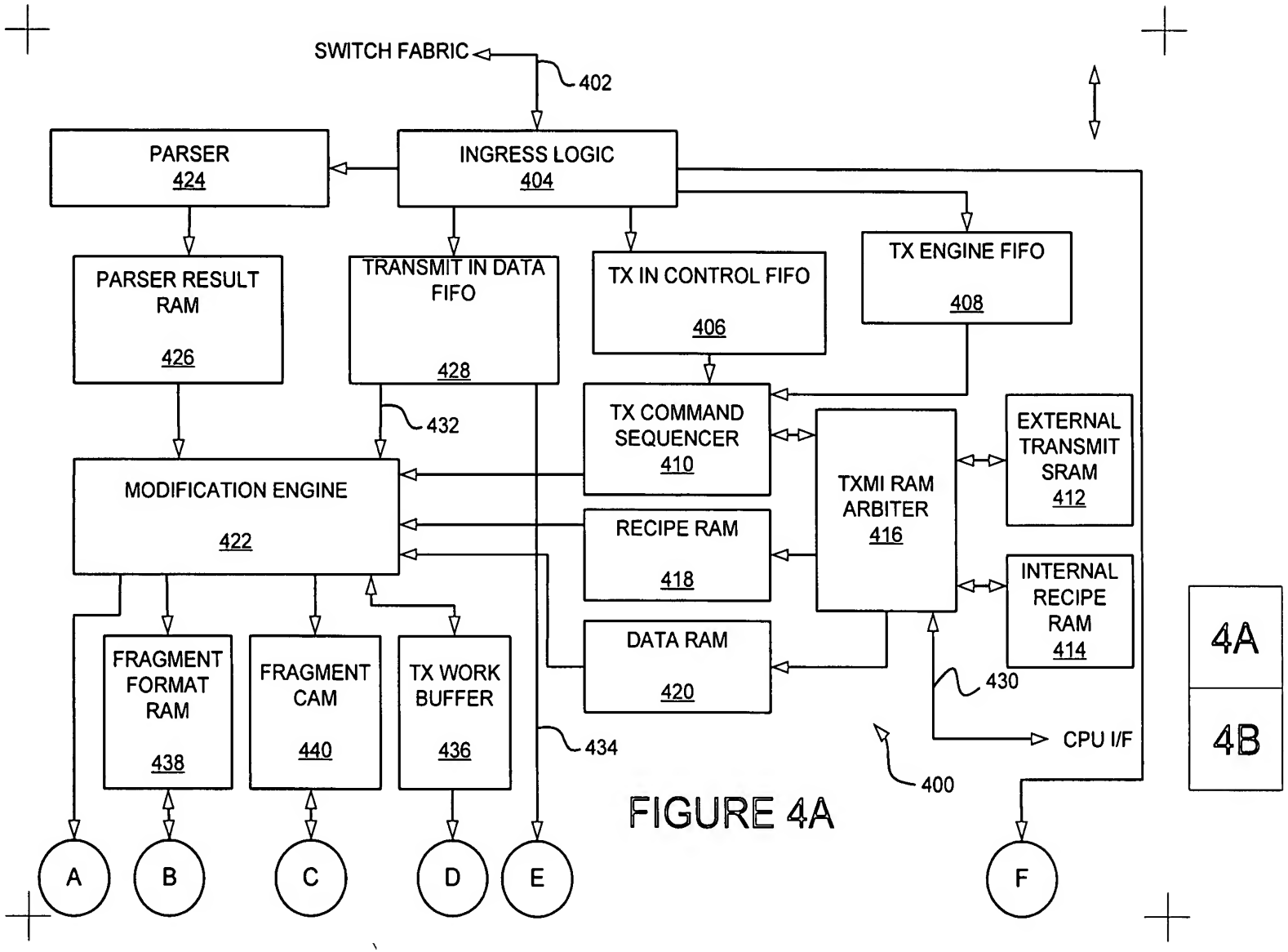

SWITCH FABRIC
402
PARSER
424
INGRESS LOGIC
404
PARSER RESULT RAM
426
TRANSMIT IN DATA FIFO
428
TX IN CONTROL FIFO
406
TX ENGINE FIFO
408
432
TX COMMAND SEQUENCER
410
TXMI RAM ARBITER
416
EXTERNAL TRANSMIT SRAM
412
MODIFICATION ENGINE
422
RECIPE RAM
418
INTERNAL RECIPE RAM
414
DATA RAM
420
430
FRAGMENT FORMAT RAM
438
FRAGMENT CAM
440
TX WORK BUFFER
436
434
CPU I/F
400
A
B
C
D
E
F
4A
4B

FIGURE 4A

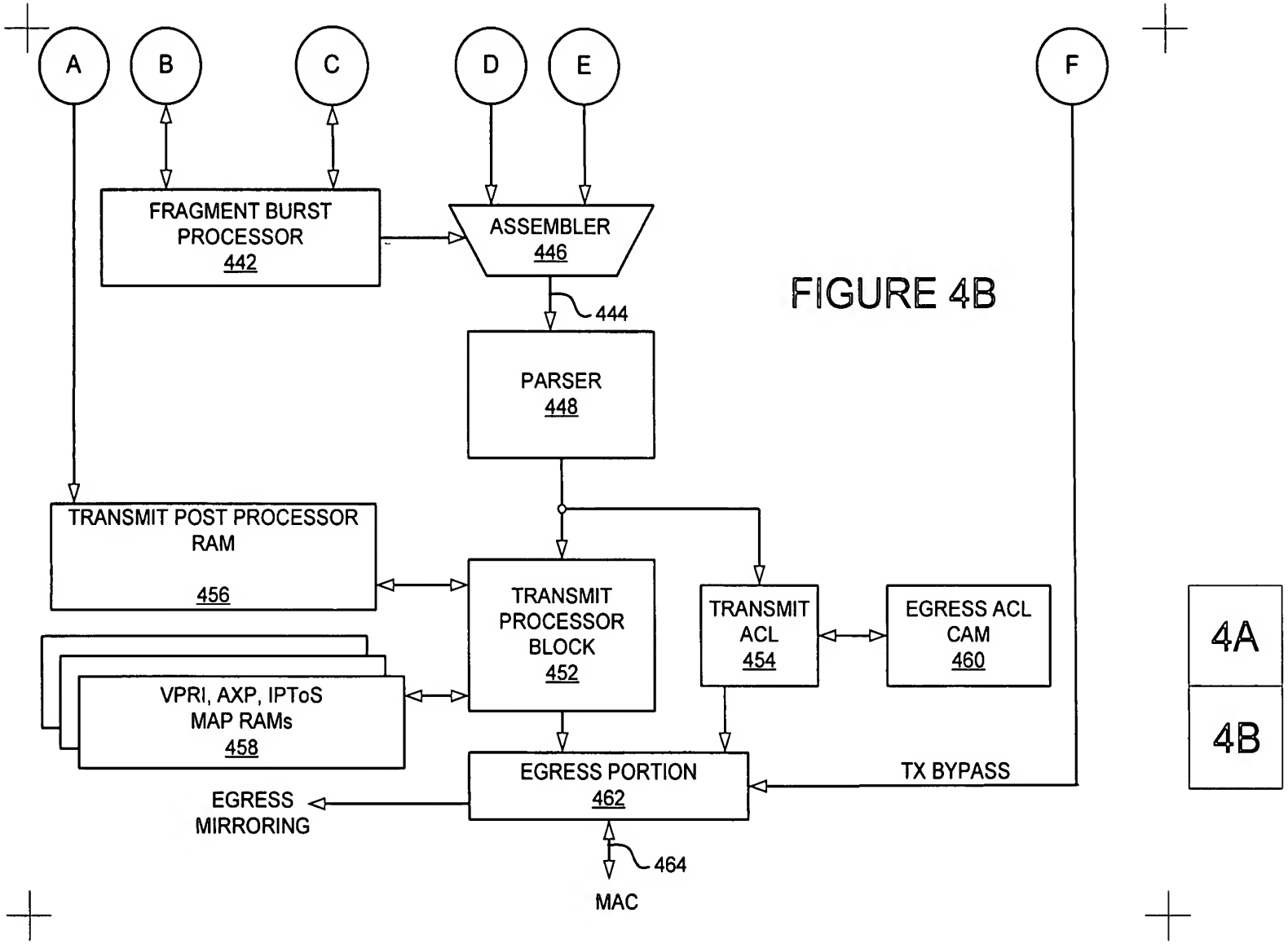

A
B
C
D
E
F
FRAGMENT BURST PROCESSOR 442
ASSEMBLER 446
444
PARSER 448
TRANSMIT POST PROCESSOR RAM 456
TRANSMIT PROCESSOR BLOCK 452
TRANSMIT ACL 454
EGRESS ACL CAM 460
VPRI, AXP, IPToS MAP RAMs 458
EGRESS PORTION 462
TX BYPASS
EGRESS MIRRORING
464
MAC
4A
4B

FIGURE 4B

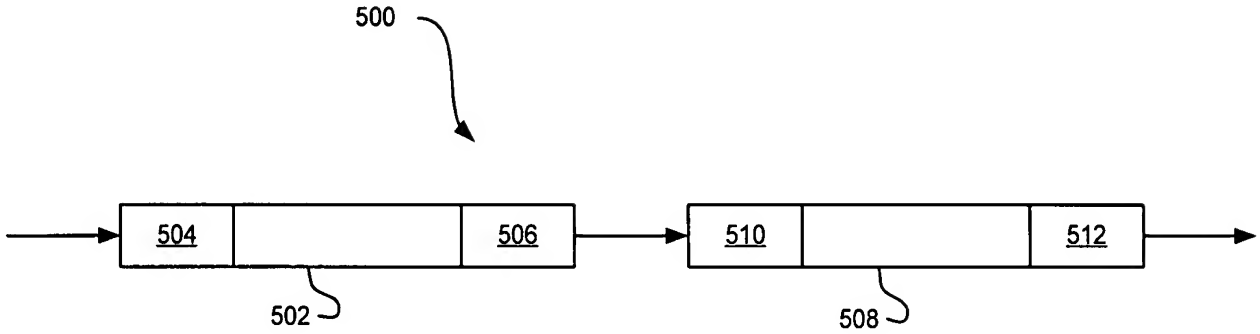


FIGURE 5

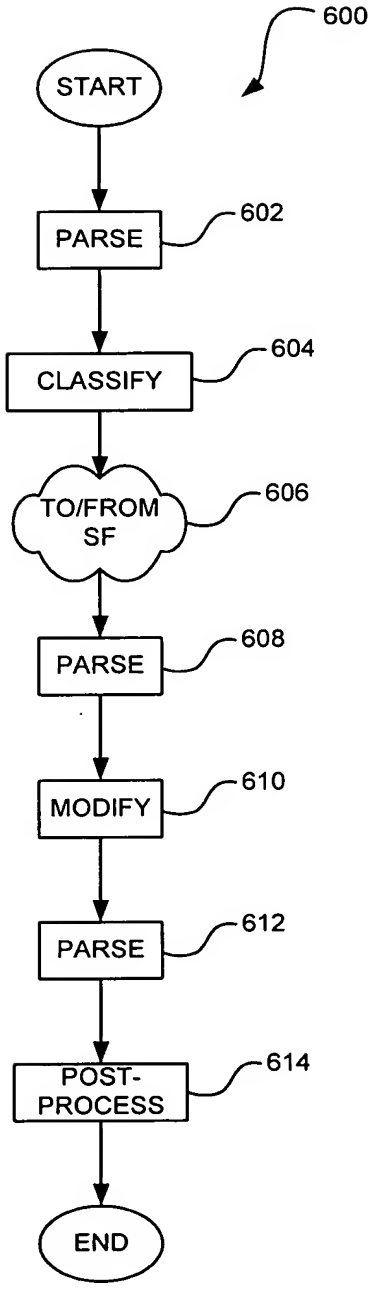

600
START
PARSE
602
CLASSIFY
604
TO/FROM SF
606
PARSE
608
MODIFY
610
PARSE
612
POST-PROCESS
614
END

FIGURE 6

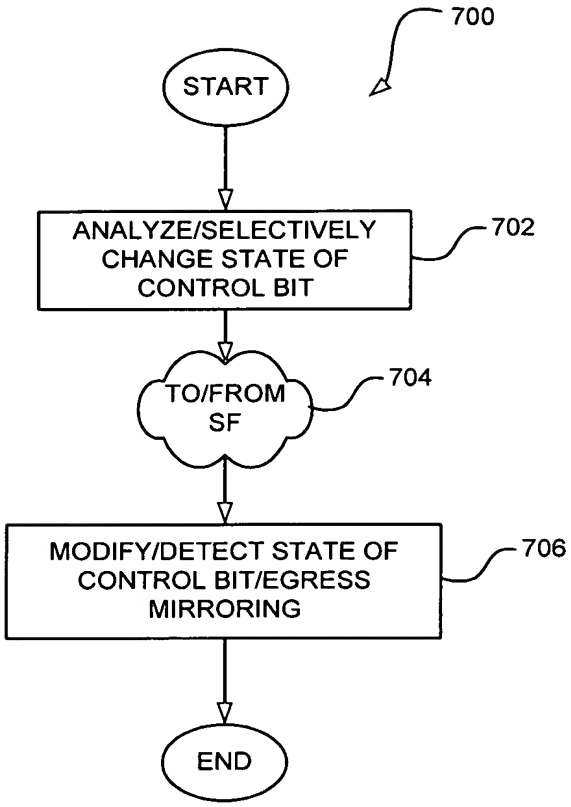

700
START
ANALYZE/SELECTIVELY CHANGE STATE OF CONTROL BIT
702
TO/FROM SF
704
MODIFY/DETECT STATE OF CONTROL BIT/EGRESS MIRRORING
706
END

FIGURE 7

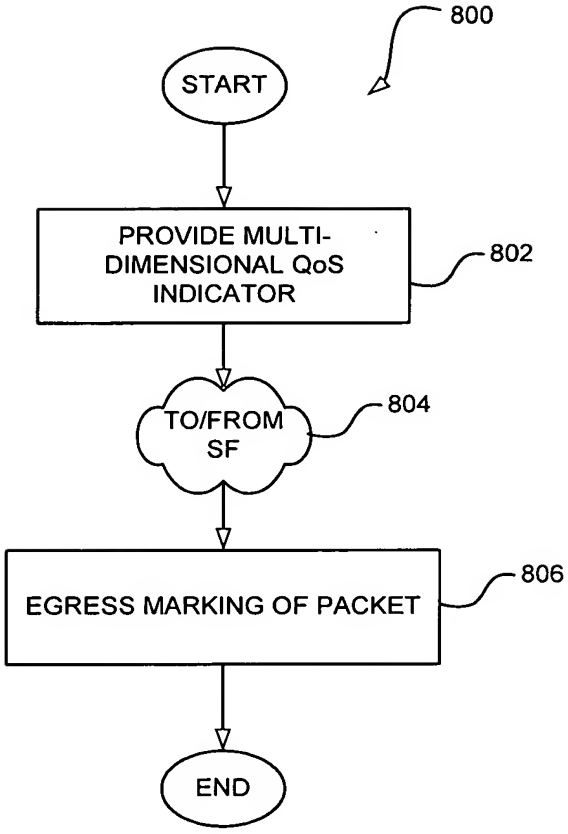

800
START
PROVIDE MULTI-DIMENSIONAL QoS INDICATOR
802
TO/FROM SF
804
EGRESS MARKING OF PACKET
806
END

FIGURE 8

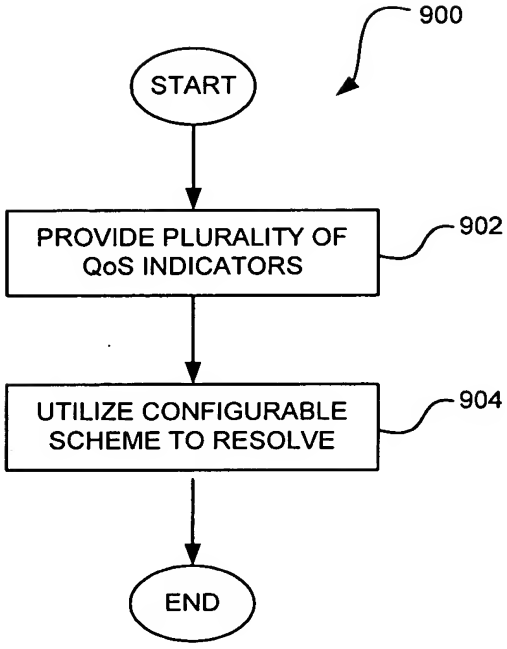

900
START
PROVIDE PLURALITY OF QoS INDICATORS
902
UTILIZE CONFIGURABLE SCHEME TO RESOLVE
904
END

FIGURE 9

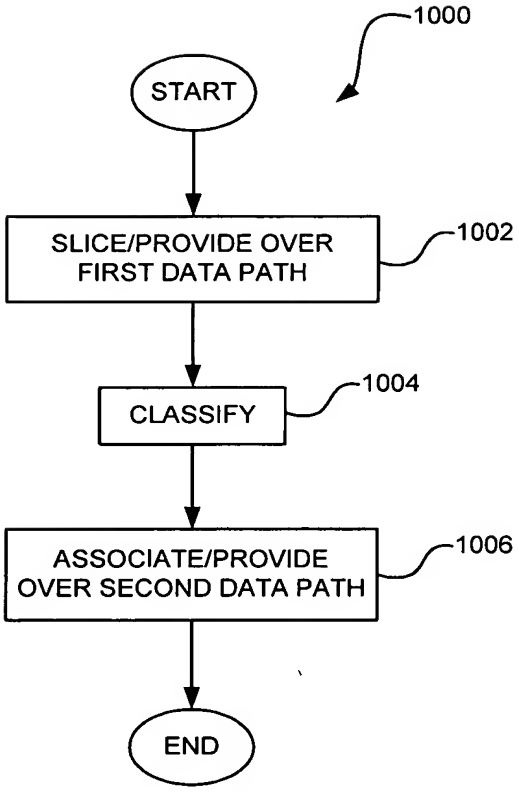

1000
START
SLICE/PROVIDE OVER FIRST DATA PATH
1002
CLASSIFY
1004
ASSOCIATE/PROVIDE OVER SECOND DATA PATH
1006
END

FIGURE 10

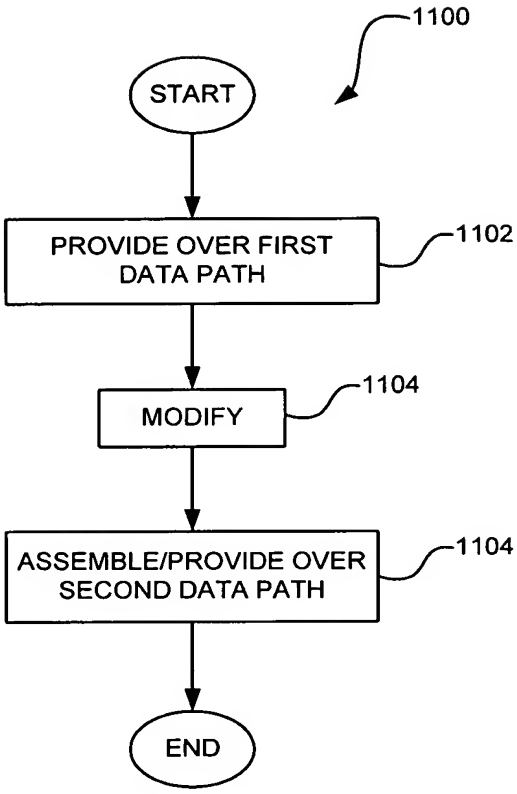

1100
START
PROVIDE OVER FIRST DATA PATH
1102
MODIFY
1104
ASSEMBLE/PROVIDE OVER SECOND DATA PATH
1104
END

FIGURE 11

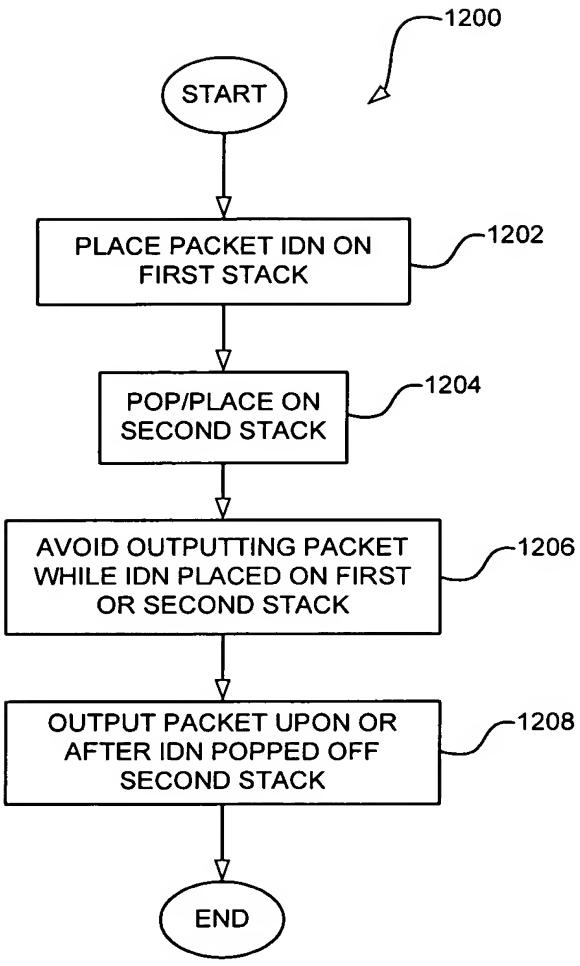

1200
START
PLACE PACKET IDN ON FIRST STACK
1202
POP/PLACE ON SECOND STACK
1204
AVOID OUTPUTTING PACKET WHILE IDN PLACED ON FIRST OR SECOND STACK
1206
OUTPUT PACKET UPON OR AFTER IDN POPPED OFF SECOND STACK
1208
END

FIGURE 12

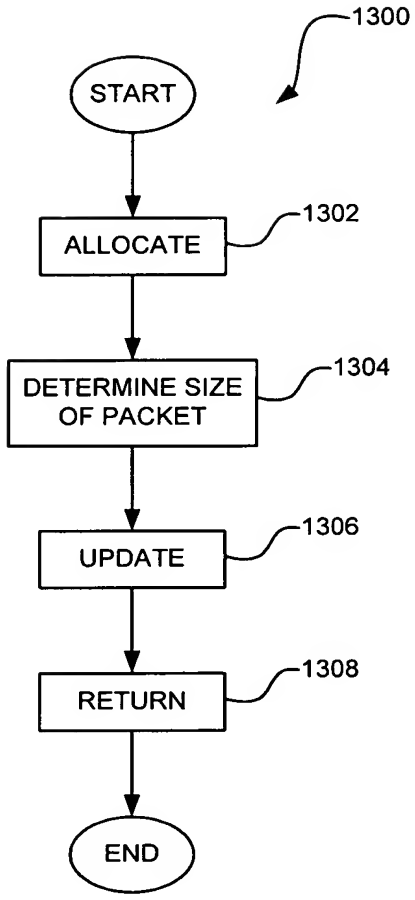

1300
START
1302
ALLOCATE
1304
DETERMINE SIZE OF PACKET
1306
UPDATE
1308
RETURN
END

FIGURE 13

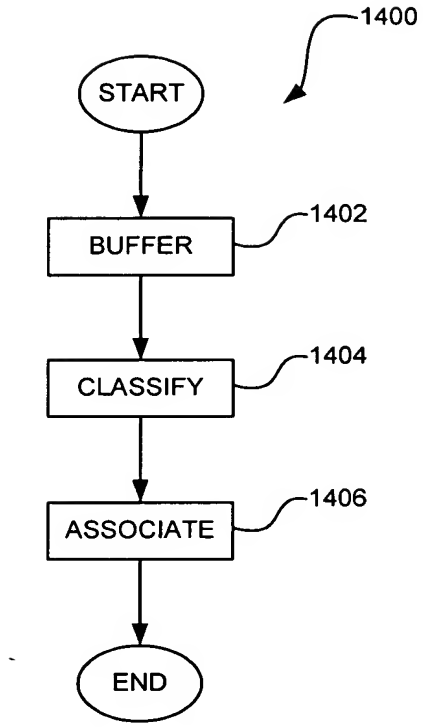


FIGURE 14

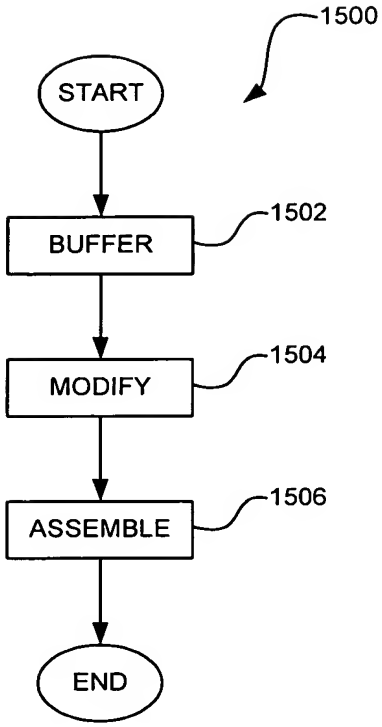


FIGURE 15

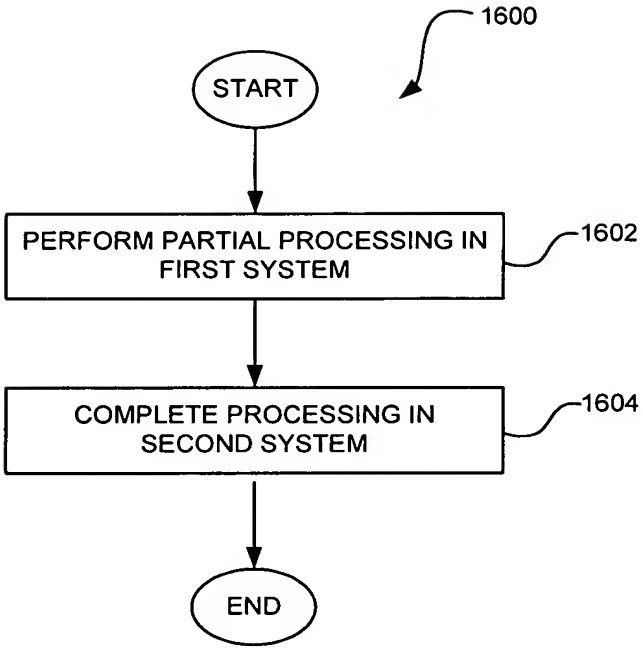

1600
START
PERFORM PARTIAL PROCESSING IN FIRST SYSTEM
1602
COMPLETE PROCESSING IN SECOND SYSTEM
1604
END

FIGURE 16

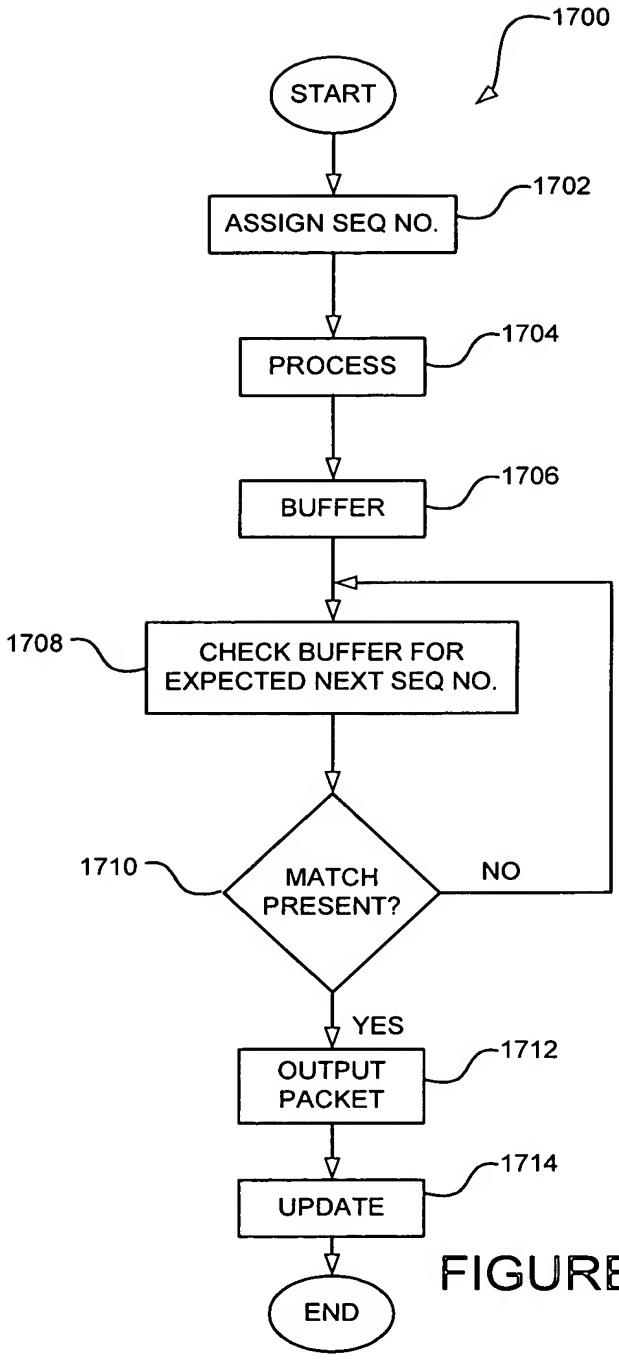

1700
START
ASSIGN SEQ NO.
1702
PROCESS
1704
BUFFER
1706
1708
CHECK BUFFER FOR EXPECTED NEXT SEQ NO.
1710
MATCH PRESENT?
NO
YES
OUTPUT PACKET
1712
UPDATE
1714
END

FIGURE 17